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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/750,373

12/31/2003

Jonathan Westphal

80001

4894

27975

7590

03/24/2005

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EXAMINER

BOUTSIKARIS, LEONIDAS

ART UNIT

PAPER NUMBER

2872

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/750,373	Applicant(s) WESTPHAL, JONATHAN	
	Examiner Leo Boutsikaris	Art Unit 2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2004.  
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 3 and 5-13 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☒ Claim(s) 5-13 is/are allowed.  
 6) ☒ Claim(s) 3 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 24 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☐ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_  
 4) ☐ Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_  
 5) ☐ Notice of Informal Patent Application (PTO-152)  
 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fellows (US 5,150,242) in view of DiJaili (US 6,853,658).

Fellows discloses an integrated optical OR device comprising electrical control inputs 5, 6, and 7, a reference optical signal 8 and an optical output Y at the face 16 which corresponds to the logical OR function of the inputs 5, 6, 7 (Fig. 1, line 35, col. 5 to line 15, col. 6). However, Fellows does not disclose an optical device that performs a logical NOR function of the electrical control inputs. DiJaili discloses a series of optical logic circuits, based on semiconductor amplifiers, wherein he teaches that an optical NOT gate can be used to invert a received optical signal (Figs. 3A-3B, lines 23-43, col. 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the NOT logic gate of DiJaili in series with the logic OR gate of Fellows, for producing an optical signal that corresponds to the logic NOR function of the electrical inputs of the Fellows device, since logic NOR gates are important building blocks in digital circuits (see lines 32-40, col. 1 in DiJaili).

***Response to Arguments***

Applicant's arguments with respect to claim 3 have been considered but are moot in view of the new ground(s) of rejection.

It is noted that output 7 in the Truth Table of col. 25-26 does not represent an output of the arrangement depicted in Fig. 21.

***Allowable Subject Matter***

Claims 5-13 are allowed.

Claims 5-13 are allowable over the prior art of record for at least the reason that even though the prior art discloses optical NOR gates, the prior art fails to teach or reasonably suggest an optical element comprising at least one combination of optical elements producing respective XOR and COIN function outputs of the two control inputs which function outputs are used in producing a logical NOR function of the two control inputs, as set forth by the claimed combination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Leo Boutsikaris whose telephone number is 571-272-2308.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leo Boutsikaris, Ph.D.

Primary Patent Examiner, AU 2872

March 18, 2005



**LEONIDAS BOUTSIKARIS  
PRIMARY EXAMINER**